

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device having a duty cycle correction circuit and an interpolating circuit interpolating a clock signal in the semiconductor memory device are disclosed. The semiconductor memory device comprises a duty cycle correction circuit, which receives an external clock, corrects the duty cycle of the external clock, and outputs the corrected duty cycle. The duty cycle correction circuit comprises a first delay locked loop that receives the external clock, inverts the external clock, synchronizes the external clock with the inverted external clock, and outputs the synchronized clock; a second delay locked loop that receives the inverted external clock, synchronizes the inverted external clock with the external clock and outputs the synchronized clock; an inverting circuit that inverts the output signal of the first delay locked loop; an interpolation circuit that interpolates the output signal of the inverting circuit with the output signal of the second delay locked loop, and outputs the interpolated signal; and a control circuit that controls the interpolation circuit in response to the clock frequency information of the external clock.